REMARKS

Summary

By this Amendment, non-elected Claims 16-23 have been canceled, Claims 7-9 have been amended, and new Claims 24-27 have been added for the Examiner's consideration.

Accordingly, Claims 7-15 and 24-27 are now pending in the application.

Claim Objections

By this Amendment, Claims 7-9 have been revised as suggested by the Examiner to change "through hall" to - - through hole - - .

35 U.S.C. ¶102

Claims 7-15 were rejected under 35 U.S.C. ¶102 as being anticipated by Fukutomi et al. (US 6268648) for the reasons stated at pages 3-6 of the Office Action.

Without acquiescing to the reasoning underlying the Examiner's rejection, Applicants respectfully traverse this rejection on the grounds that Fukutomi et al. is not prior art against the claims of the present application.

That is, the present application is a Divisional of application Serial No. 09/062,720, filed April 20, 1998. Accordingly, the claims of the present

application are entitled to a U.S. filing date of April 20, 1998, which is prior to both (a) the ¶102(e) date of Fukutomi et al. of October 29, 1999, and (b) the PCT publication date of the counterpart International application of November 5, 1998.

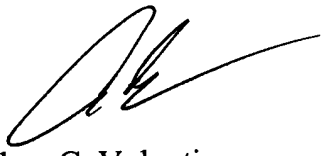
Accordingly, withdrawal of the rejection based on Fukutomi et al. is respectfully requested.

Conclusion

No other issues remaining, reconsideration and favorable action upon the Claims 7-15 and 24-27 now-pending in the application are requested.

Respectfully submitted,

TAKAAKI SASAKI

By: 

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ATTACHMENT "A"

Additions/Deletions to Claims 7-9:

7. (Amended) A method of manufacturing a semiconductor device with a semiconductor element fixed to a semiconductor package, comprising the steps of:

preparing said semiconductor package structured by providing a substrate for mounting said semiconductor element thereon to fix said semiconductor element to one side thereof and a connecting pattern provided on the other side of said substrate and by forming a through [~~hall~~] hole from the one side to the other side of said substrate;

fixing a surface where the element is formed of said semiconductor element on the one side of said substrate of said semiconductor package such that an electrode of said semiconductor element is within said through [~~hall~~] hole;

electrically connecting said connecting pattern and said electrode of said semiconductor element via wires through said through [~~hall~~] hole; and

sealing said through hall and said wires with resin.

8. (Amended) A method of manufacturing a semiconductor device as claimed in claim 7, wherein said connecting pattern is provided continuously in a plurality of stages and an end portion of said connecting pattern on the side of said

through [~~hall~~] hole is provided on a stage on the side of the one said of said substrate.

9. (Amended) A method of manufacturing a semiconductor device as claimed in claim 7, wherein said through [~~hall~~] hole is a plurality of through [~~halls~~] holes.